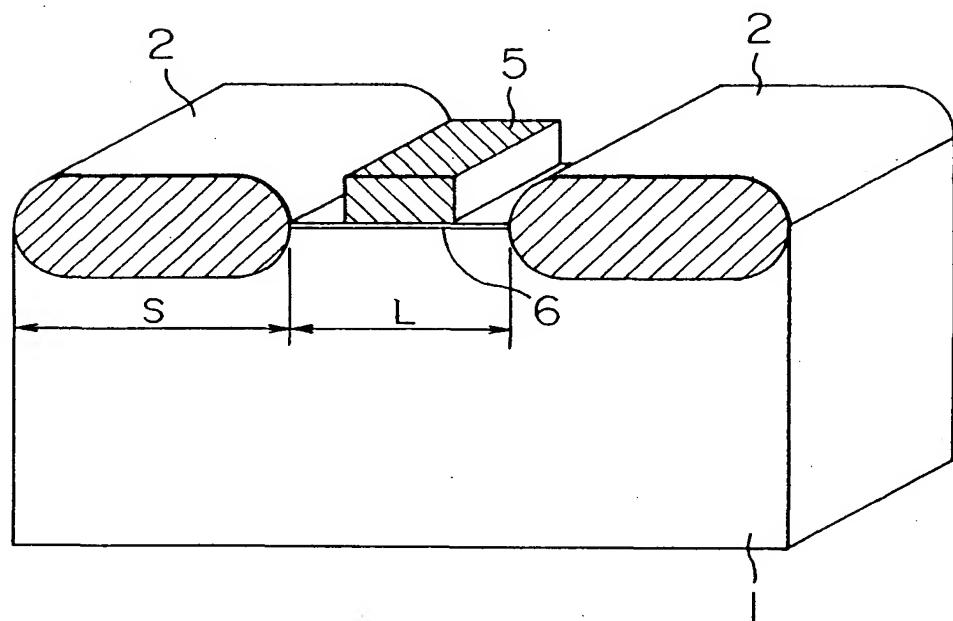


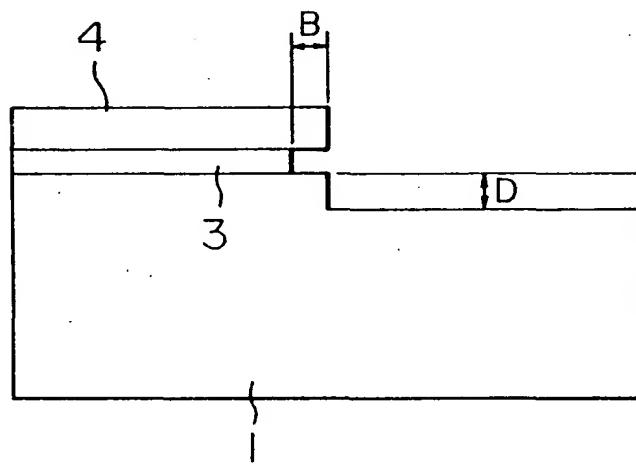
F I G. 1

THREE-DIMENSIONAL LOCOS SHAPE

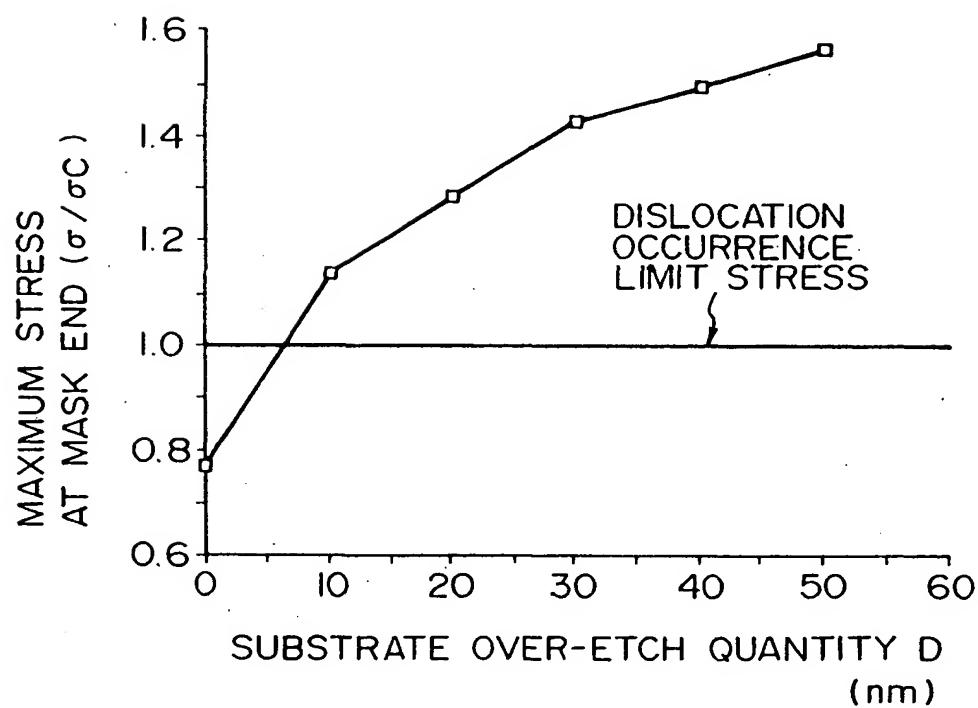


F I G . 2A

EXAMPLE OF ANALYSIS OF STRESS INCREASING CONDITION
AT THE TIME OF FORMATION OF GROOVE

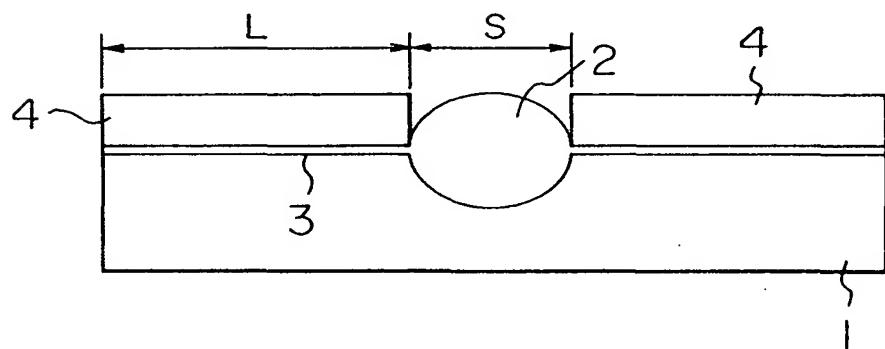


F I G . 2B



F I G. 3A

EXAMPLE OF ANALYSIS SHOWING DEPENDENCE
OF RESULTING STRESS ON L/S DIMENSION



F I G. 3B

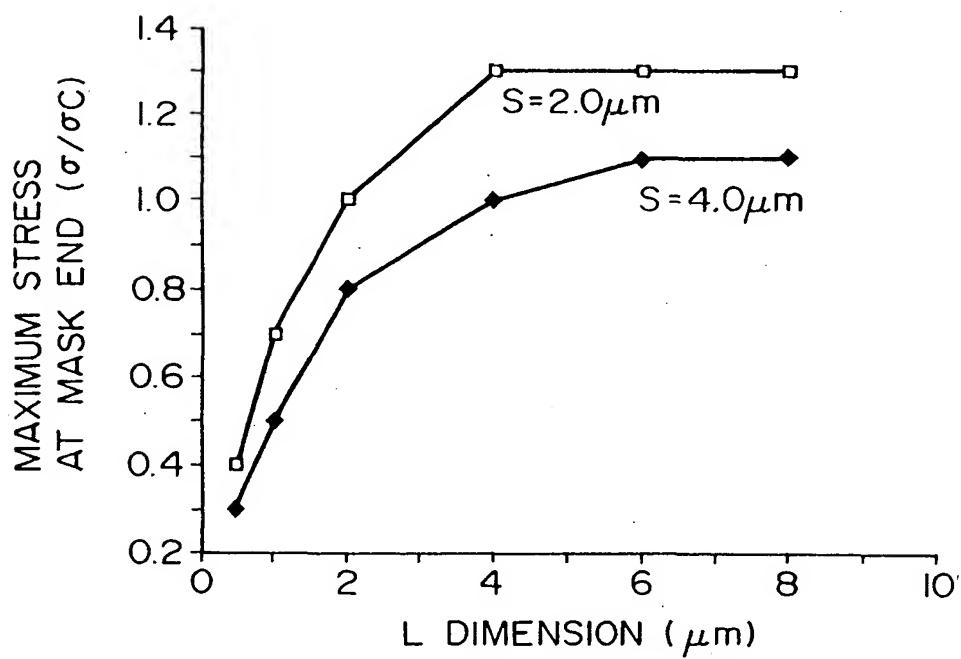


FIG. 4
EXAMPLE OF DESIGN CHART

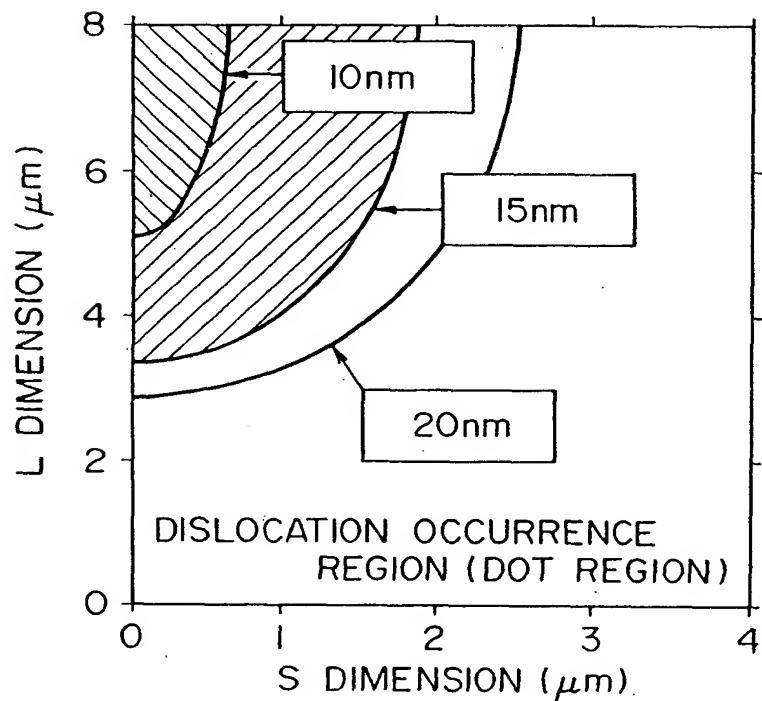
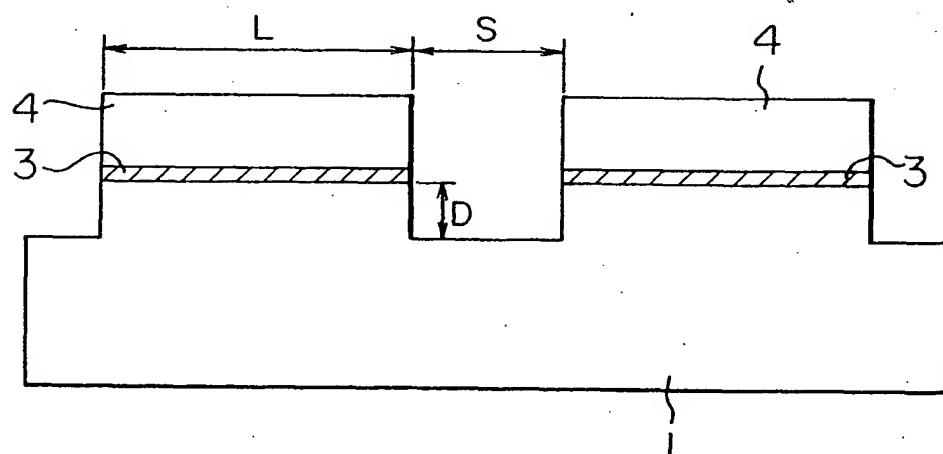
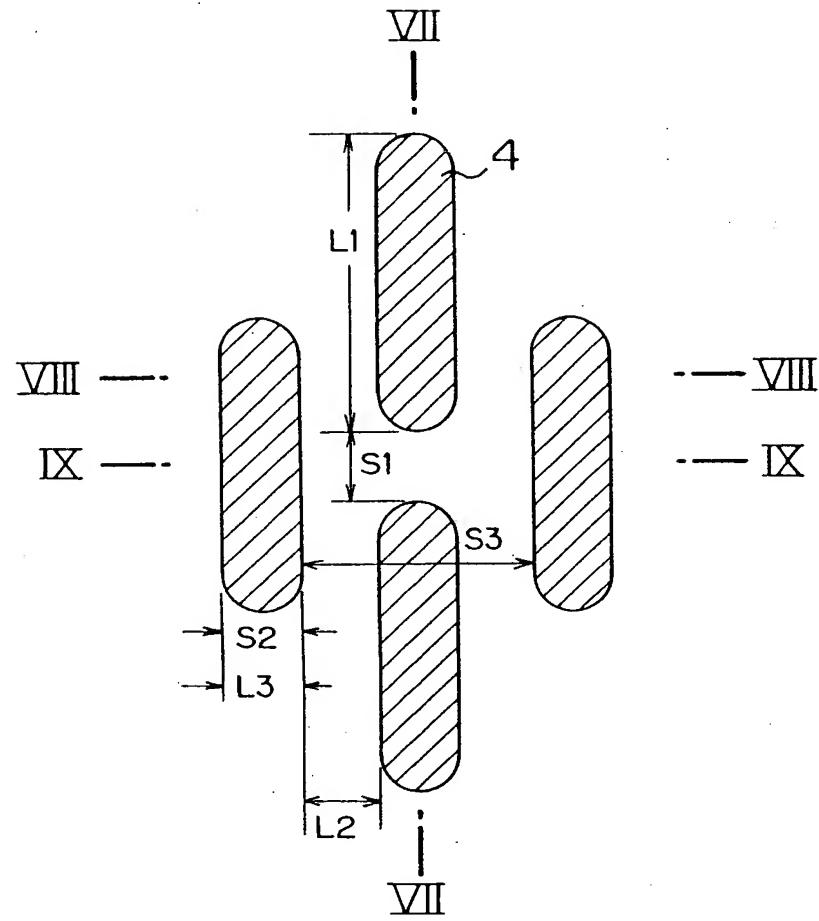


FIG. 5
SECTIONAL VIEW IN DEVICE ISOLATION STEP



F I G . 6
PLAN VIEW WHEN FORMING DEVICE ISOLATION REGION



F I G . 7
SECTIONAL VIEW TAKEN ALONG LINE VII-VII OF FIG. 6

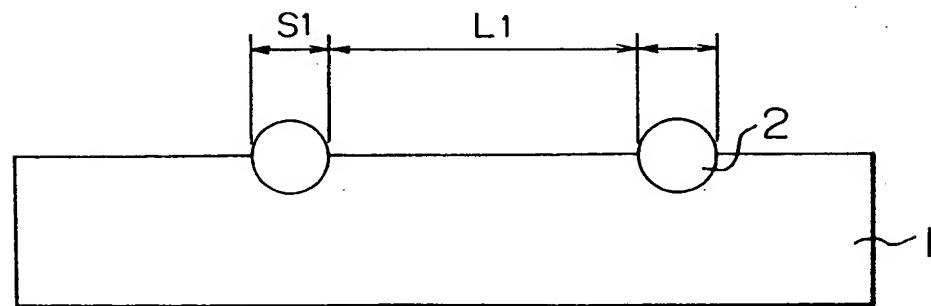


FIG. 8

SECTIONAL VIEW TAKEN ALONG LINE VIII-VIII OF FIG.6

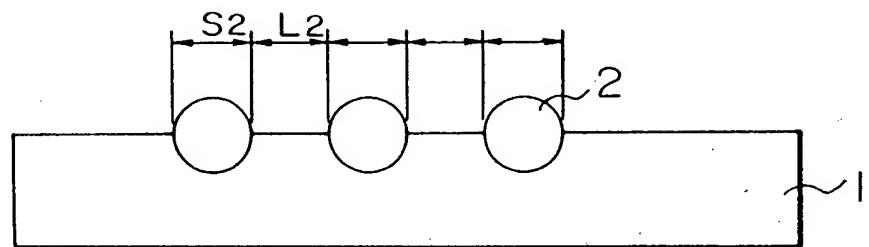


FIG. 9

SECTIONAL VIEW TAKEN ALONG LINE IX-IX OF FIG.6

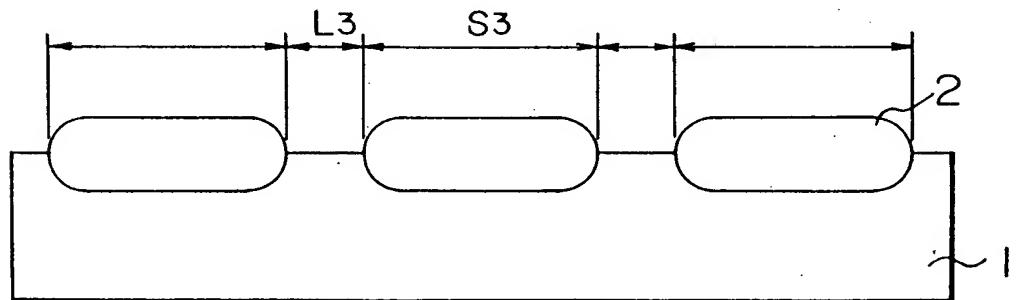


FIG. 10

FLOW FOR DETERMINING WIDTH DIMENSION OF DEVICE FORMATION REGION OR DEVICE ISOLATION REGION

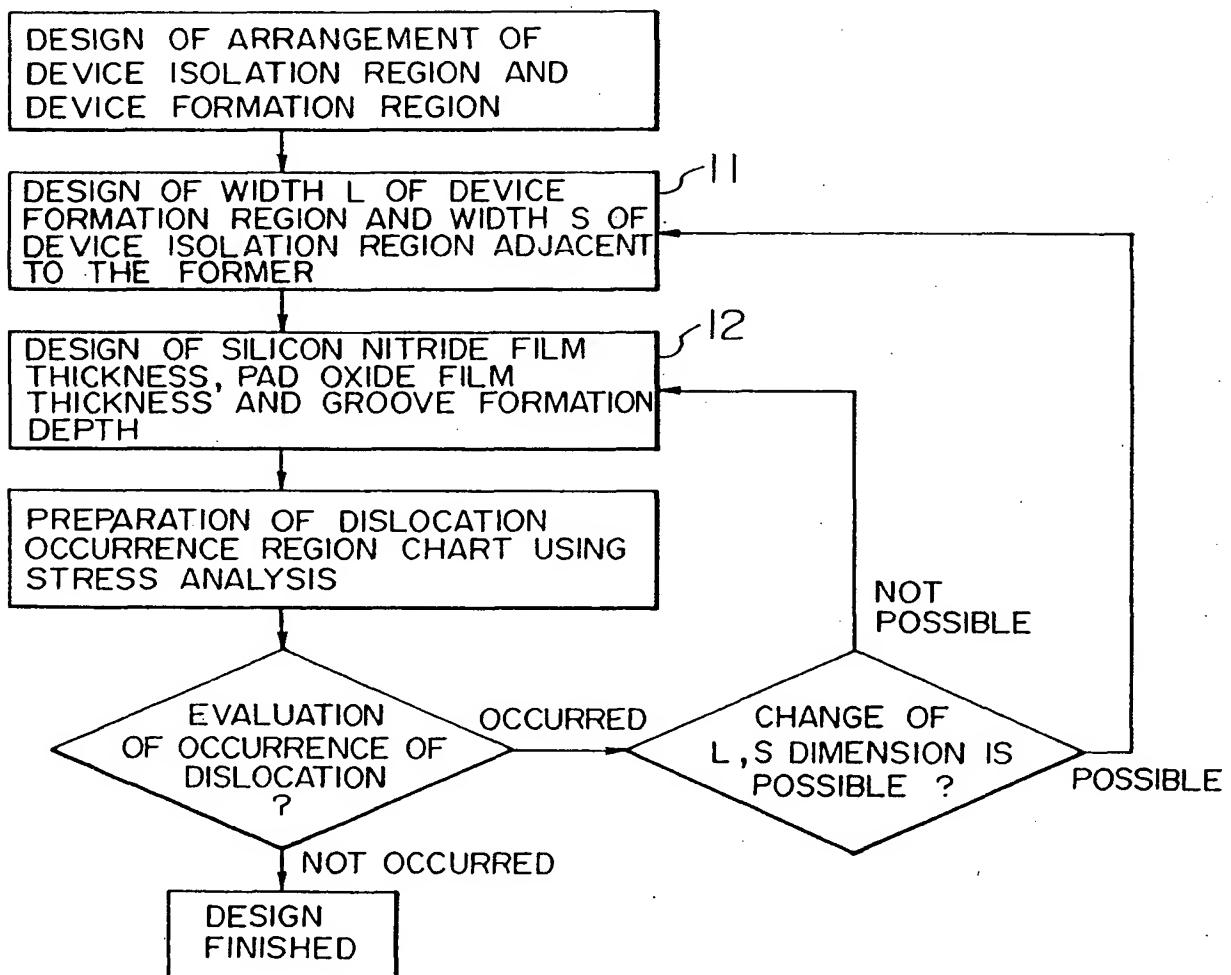
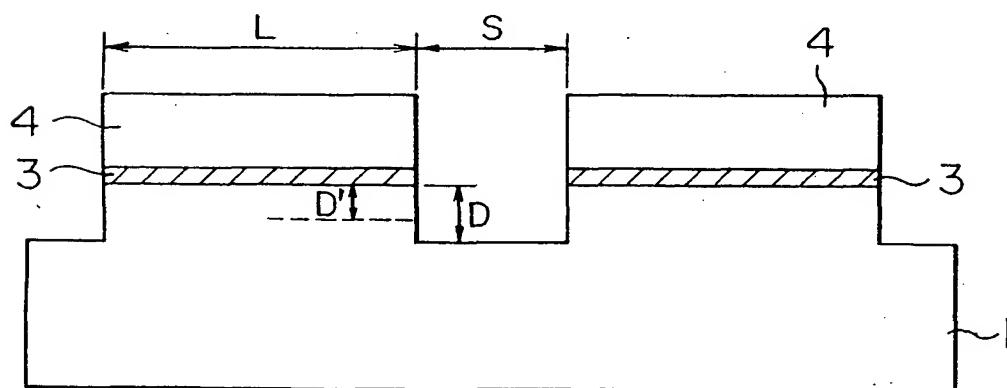


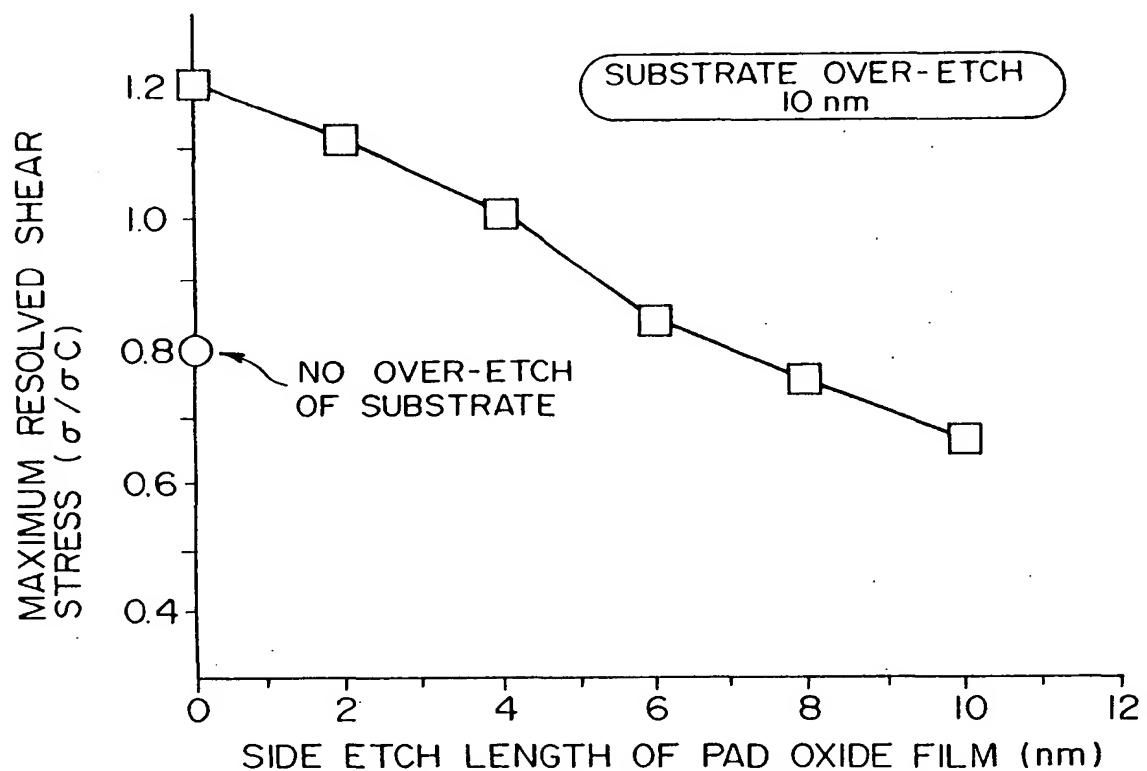
FIG. 11

SECTIONAL VIEW OF SEMICONDUCTOR DEVICE AFTER GROOVE FORMATION



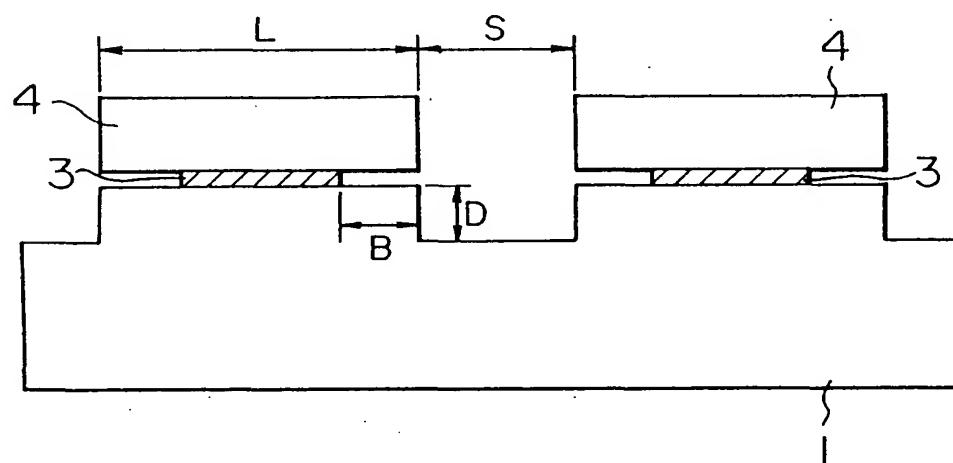
F I G. 12

RELATION BETWEEN ETCH-BACK DISTANCE OF PAD OXIDE FILM
AND MAXIMUM STRESS NEAR GROOVE END



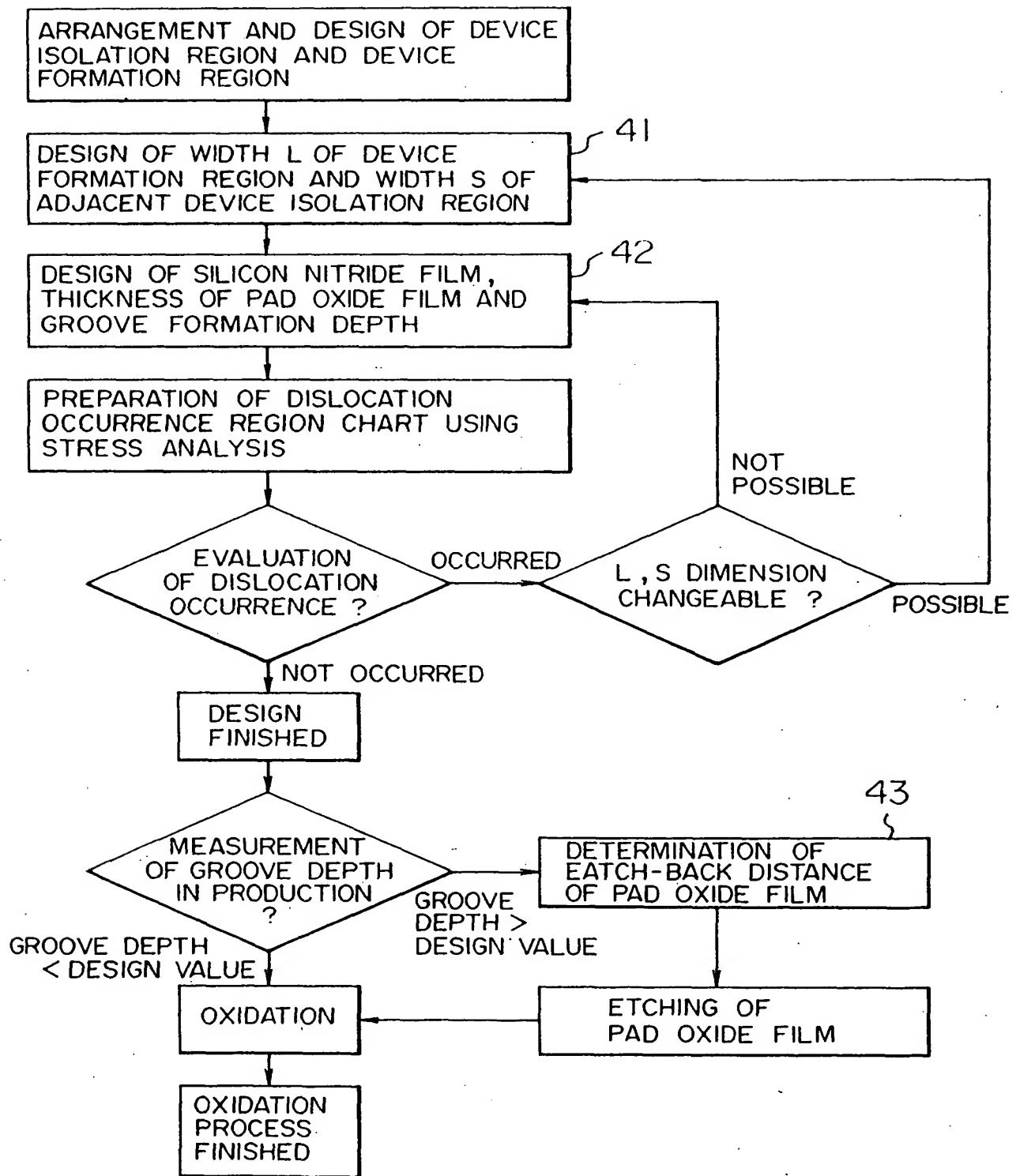
F I G. 13

SECTION OF DEVICE AFTER ETCH-BACK OF PAD OXIDE FILM



F I G. 14

FLOW FOR DETERMINING WIDTH OF DEVICE FORMATION REGION OR DEVICE ISOLATION REGION



F I G. 15

MICROGRAPH OF SEMICONDUCTOR CRYSTAL STRUCTURE SHOWING FORMATION EXAMPLE OF DEVICE ISOLATION REGION

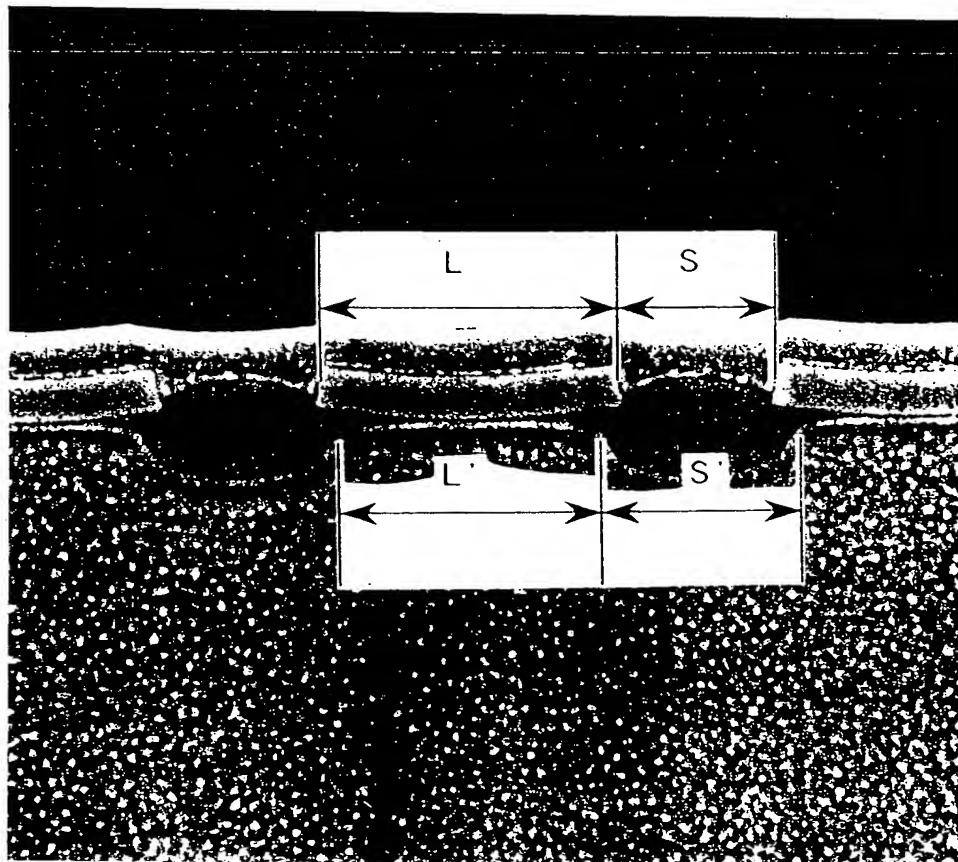


FIG. 16

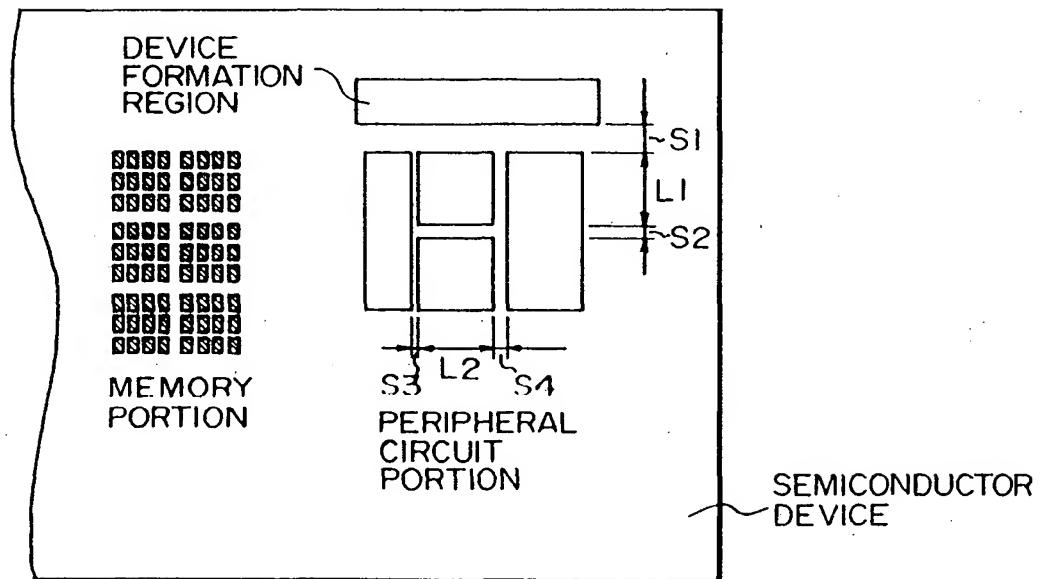
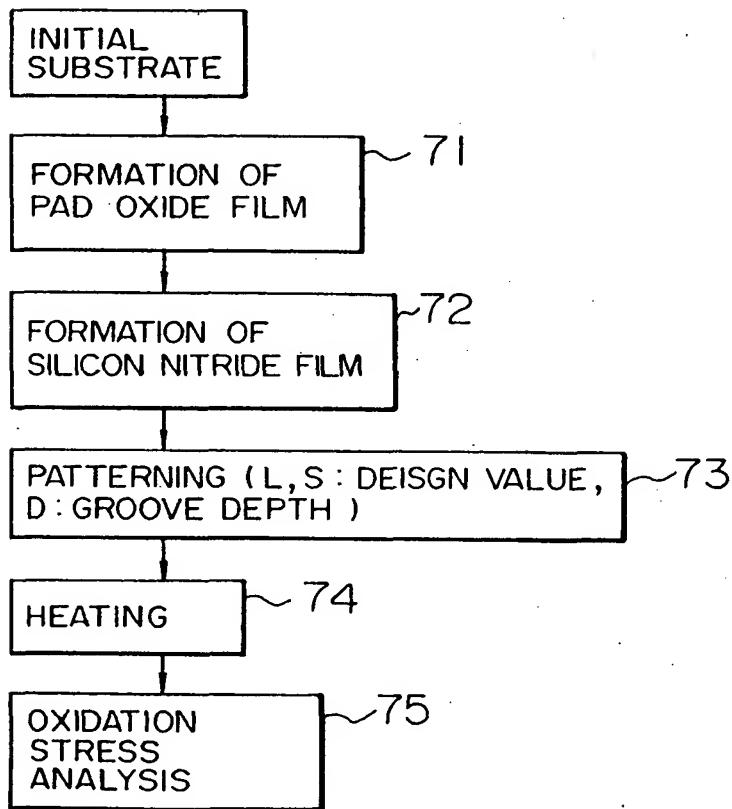
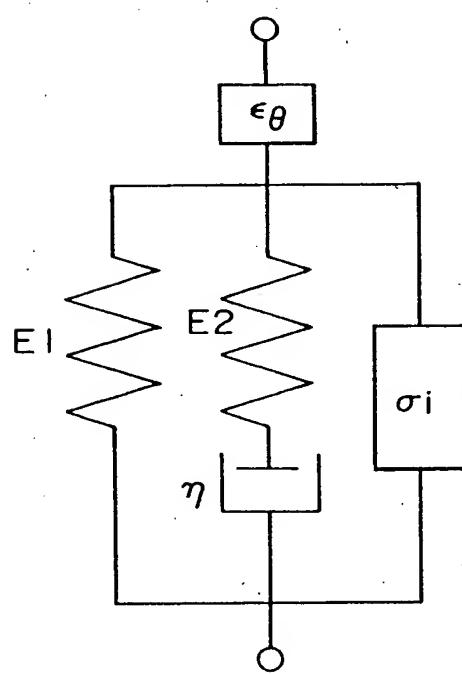


FIG. 17

STRESS ANALYSIS STEP



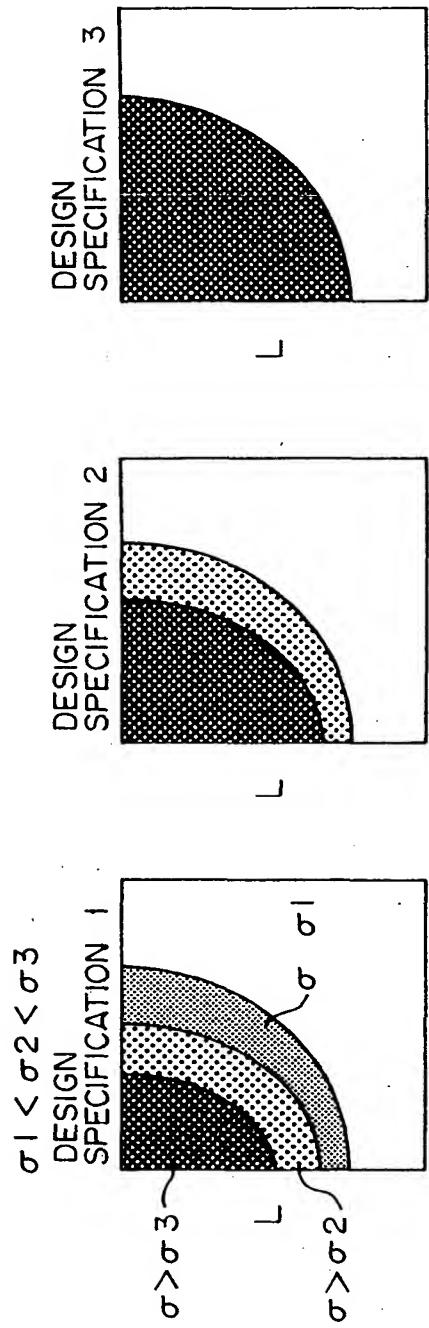
F I G. 18



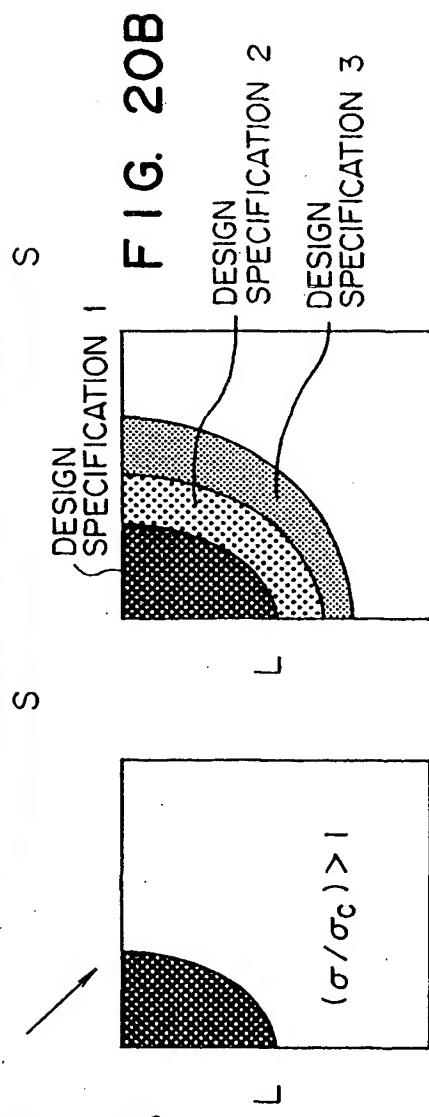
VISCO-ELASTIC MODEL FOR STRESS ANALYSIS

STRESS DISTRIBUTION CHART OF EACH SPECIFICATION

FIG. I9C FIG. I9B FIG. I9A



S FIG. 20A



**DESIGN CHART OF
DESIGN SPECIFICATION 1**

**COLLECTIVE
DESIGN CHART**

S

S

DOT REGION : ($\sigma / \sigma_C > 1$)

F I G . 21

